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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,912	06/30/2000	Douglas E. Duschatko	M-8320 US	1177

33031 7590 10/28/2003

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EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	9

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

H.R

Office Action Summary

Application No.	Applicant(s)
09/607,912	Duschatko et al.
Examiner	**Art Unit**
Man Phan	2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 30, 2000*

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1 and 4-10* is/are rejected.

7) ☒ Claim(s) *2, 3, 11, and 12* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Mar 30, 2000* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The application of Duschatko et al. for a "Path AIS insertion for concatenated payloads across multiple processors" filed 06/30/2000 has been examined. This application claims benefit from Provisional Application 60/211,559 dated 06/15/2000. Claims 1-12 are pending in the application.

Specification

2. The disclosure is objected to because of the following informalities:

The status of the related US Patent application noted on pages 1, 2 and 4 need to be updated. Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Reference character (140) as shown in Fig. 1A.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "CDR 1300" (as shown in Fig. 5) and "CDR 500"(as described in pages 17-18 for Fig. 5) have both been used to designate (CDRs).

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because

reference characters "Line Card 1310" (as shown in Fig. 5) and "Line Card 510"(as described in pages 17-18 for Fig. 5) have both been used to designate Line Cards.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 1 is objected to because of the following informalities: On line 2, "concentrated signals" should be --concatenated signals--.. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 4-6 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baydar et al. (US#5,717,693) in view of Derbenwick et al. (US#6,262,975).

With respect to claims 1, 4-6 and 7-10, both Baydar et al. (US#5,717,693) and Derbenwick et al. (US#6,262,975) disclose a novel method and system for quickly generating and transmitting SONET AIS signals according to the essential features of the claims. Baydar discloses a SONET payload pointer processing and its transport overhead architecture. Figs. 1a&b block diagrams illustrated a SONET pointer processing integrated circuit, comprising a demultiplexer (4nq) having an input for coupling to the payload and having plurality of outputs (4np); a multiplexer (4g) having a plurality of inputs; a plurality of pointer processors (4b, c), each having an input coupled to the respective input of the multiplexer, wherein each of the pointer processors comprises a bidirectional terminal coupled to a common node (Col. 3; lines 29 plus and Col. 6, lines 20 plus). Baydar further teaches in Fig. 20 illustrated the VT (Virtual Tributary structures - sub-STS mapping uses in SONET standard) elastic store counters, in which each of the 28 counters 463a is incremented in its VT time slot by a hard-wired pulse on a line 463c from a demultiplexer 463d which is responsive to the VT# (TRADR) signal on the line 2i and to an enable (EN) signal on a line 463e. VT alarm registers block 350 stores two alarm signals for each independent VT pointer. VT path AIS on the line 346 and VTLOP on a line 470 are stored into flip-flops synchronously in the corresponding VT time slots. Once these flip-flops are set, they are not reset until they are read. They are read out on a line by the microprocessor interface as 4-bit groups carrying information for two VTs. If one of the VT path AIS or VTLOP bits is active, a VT error is generated and stored in a separate register set whose outputs are provided on a line 474 and multiplexed with the tributary addresses in a VT Data Multiplexer of a VT pointer generation block 476 shown

in Fig. 4D and Fig. 31b in detail (Col. 19, lines 60 plus).

However, Baydar does not expressly disclose the circuitry for causing a logic level to be asserted at the common node in response to an error signal at the processor input, and wherein the alarm means is included as a component of a concatenated payload. In the same field of endeavor, Derbenwick et al. discloses a method for auditing cross-connection provisioned to carry a concatenated signal in a optical transport system, in which the incoming signals are monitored and the outputting of a signal is blocked if the pattern of output channels assigned to that signal is not correct. This is particularly useful for ensuring that a concatenated signal in a SONET transport system is transported correctly over contiguous channels. Specifically, the Derbenwick teach the process for detecting different trigger states associated with the processing of a particular incoming signal, and responsive to detecting the presence of one of the trigger states and responsive to a determination that the incoming signal is of a particular type, then the process determines if a pattern of outputs paths specified for the incoming signal meet a predetermined criterion and inserts an alarm signal in the specified output paths in place of the incoming signal if the predetermined criterion is not met. Advantageously, then, the Derbenwich's invention allows a communications system to output a concatenated signal only when contiguous channels have been assigned to that signal (See Fig. 5; Col. 1, lines 65 plus and Col. 4, lines 48 plus).

One skilled in the art would have recognized the need for effectively and efficiently providing a method and system for quickly generating and transmitting SONET AIS signals when pointer processor detects a fault in a concatenated payload

signal, and would have applied Derbenwick's novel use of the auditing process that provisioned to carry a concatenated signal into Baydar's overhead pointer processing for a synchronous optical network (SONET). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Derbenwick's method of auditing cross-connections related to concatenated signals in SONET into Bardar's SONET payload pointer processing and architecture with the motivation being to provide a method and system for the generation of a path alarm insertion signal (AIS) at the output of concatenated pointer processors.

Allowable Subject Matter

4. Claims 2-3 and 11-12 are objected to as being dependent upon the rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

6. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest the steps wherein the bidirectional terminal of each of the plurality of processors is coupled to the common node and the common node is coupled through a resistance to a voltage V+, so that in the absence of an alarm signal at all the processor inputs, the voltages at the bidirectional terminals of the processors approaches V+, and wherein as a result of an error signal at the input of any processor, the voltages at the bidirectional terminals of all the processors

approach a reference voltage, as specifically recited in claims 2, 3; wherein the alarm means comprises an error detector, a wired-OR logic element coupled between the error detector and the bidirectional terminal; and a combinational logic element having inputs respectively coupled to the output of the processor, as specifically recited in claim 11.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Afferton et al. (US#6,452,906) is cited to show the fault detection and isolation in a SONET and in a SDH network.

The Parruck (US#5,265,096) is cited to show the SONET alarm indication signal transmission method and apparatus.

The Kremer et al. (US#5,442,620) is cited to show the apparatus and method for preventing communications circuit misconnections in a bidirectional line-switched ring transmission system.

The Chaudhuri (US#6,324,162) is cited to show the path-based restoration mesh

networks.

The Mochizuki et al. (US#6,122,249) is cited to show the ADM apparatus.

The Chan et al. (US#6,301,254) is cited to show the virtual path. ring protection method and apparatus

The Teodorescu et al. (US#6,608,844) is cited to show the OC-3 delivery unit, timing architecture

The De Moer et al. (US#6,147,968) is cited to show the method and apparatus for data transmission in SONET.

The Martin et al. (US#6,298,038) is cited to show the transparent transport.

The Nelson et al. (US#6,421,323) is cited to show the method and apparatus for analyzing events in a telecommunications system.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (703)305-1029. The examiner can normally be reached on Mon - Fri from 6:30 to 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is (703)305-3988.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

12. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 305-9051, (for formal communications intended for entry)

Or: (703) 305-3988 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Mphan

10/20/2003.